AMENDMENTS TO THE FIGURES

Figure 1 (REPLACEMENT SHEET) has been amended by the addition of a notation to indicate that it is "PRIOR ART".

Figure 3 (REPLACEMENT SHEET), already containing a notation indicating that it is "PRIOR ART", has been amended (e.g., with enlarged dots at intersecting line connection points) to clarify the interconnections between the transistors within the master and slave latches therein.

Figure 5 (REPLACEMENT SHEET), illustrating an exemplary embodiment of the invention, has been amended (with enlarged dots at intersecting line connection points) to clarify the interconnections between the transistors within the master and slave latches disclosed therein.